WHITE PAPER

Taking Wireless Infrastructure Systems Design from 3G to 5G and Beyond

MathWorks®

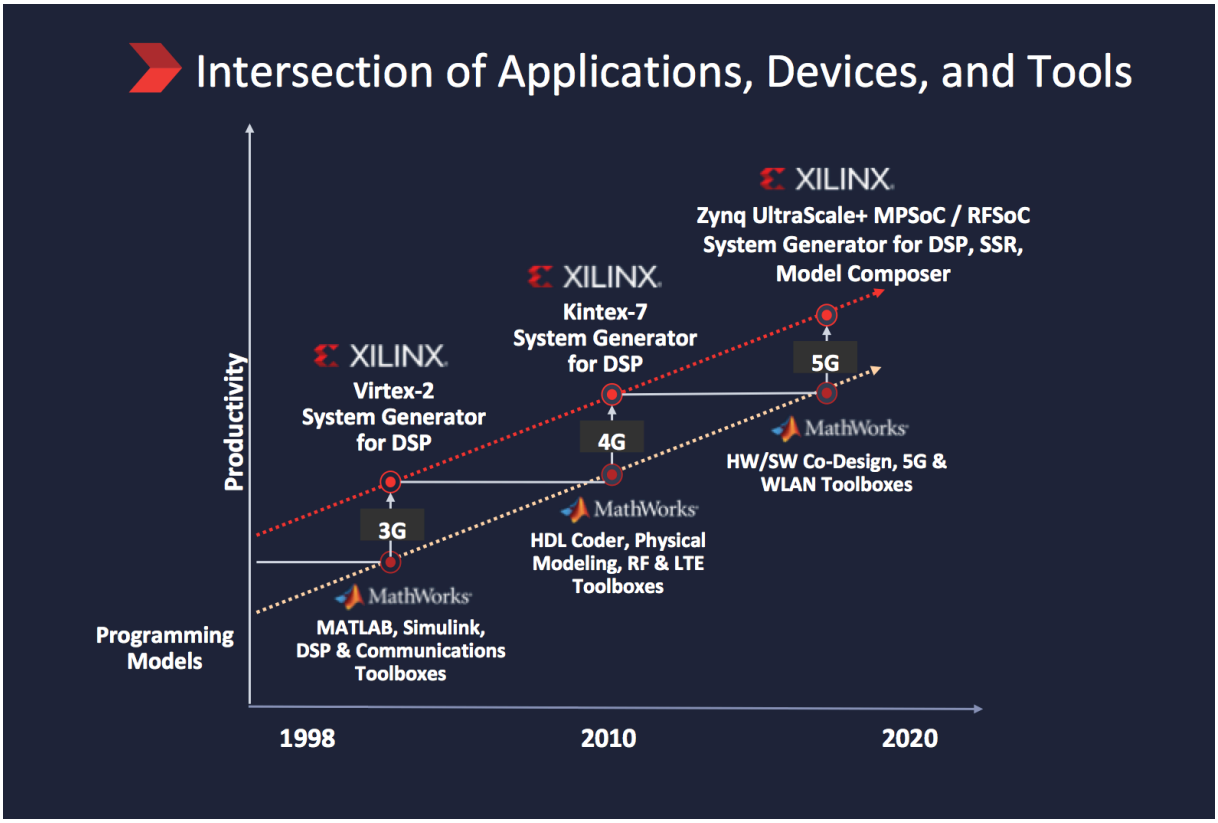
When R&D teams combine field programmable gate arrays (FPGAs) with Model-Based Design, they improve productivity, reduce time-to-market, and deliver higher quality products.

Today's FPGAs offer speed, low power consumption, and the flexibility to adapt to rapidly changing technical requirements. Originally simple interface devices featuring thousands of configurable logic blocks, they have evolved into sophisticated system-on-chips (SoCs) with millions of gates, multiple processor cores, DSP blocks, memory blocks, and interfaces. A new class of Xilinx® FPGA devices for wireless infrastructure features GHz clock speeds, multiple processor cores, RF converters and forward error correction blocks, and adaptable hardware that enables custom memory hierarchies.

Communications systems organizations invest in Model-Based Design because it is a model-centric approach to communication systems development. It uses a system model for design, analysis, simulation, automatic code generation, and verification. The system model serves as an executable specification. Teams can simulate the model at any stage to get an instant view of system behavior and to test out multiple what-if scenarios—without risk, delay, or costly re-spins. They can refine the system-level models with implementation details and continuously integrate to avoid late surprises.

This paper shows why combining Model-Based Design with FPGAs has been a game-changer for wireless infrastructure development. It traces the evolution of Xilinx FPGAs and Model-Based Design with MATLAB® and Simulink® across three generations of wireless infrastructure standards and shows how wireless communication companies are combining FPGAs with Model-Based Design to deliver high-quality products that meet 3G, 4G, and 5G standards.

> "Having MATLAB and Simulink so tightly integrated with the Xilinx toolset is a real asset for Sandia. We are so impressed with the tools and the direction in which MathWorks and Xilinx are going that we plan to make this our mainstream DSP design flow."
>
> — *Dale Dubbert, Sandia National Labs*

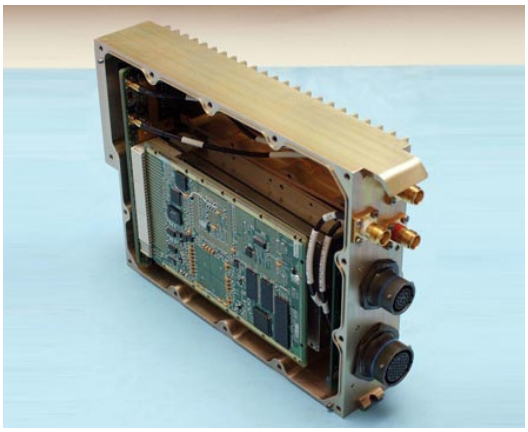


3G: Automating A Manual Process

The 3G standard featured much higher bandwidths than 2G, as well as data rates of up to 2MBPS--roughly 30 times faster than 2G. As a result, designing a 3G system became too complex and challenging for a manual approach. Before the introduction of 3G standards, a team would typically begin a project by developing an algorithm and system architecture in MATLAB and Simulink. The design would then be handed off to a hardware designer, who had to manually translate the Simulink blocks into RTL code, a process that was tedious, time-consuming, and prone to errors.

Anticipating the need for increased automation, MathWorks developed toolboxes for DSP and communications applications while Xilinx developed System Generator for DSP™, which automatically converts the Simulink design directly into RTL code and produces optimized, high-quality results. This new workflow enabled developers to automatically generate C and HDL code that matched the original model and eliminated the need for manual translation.

Case Study: BAE Systems



"It took 645 hours for an engineer with years of VHDL coding experience to hand-code a fully functional SDR waveform using our traditional design flow. A second engineer with limited experience completed the same project using Simulink and Xilinx System Generator in fewer than 46 hours."

— *Dr. David Hessig, BAE Systems*

BAE Systems was tasked with developing a military standard satellite communications waveform for implementation in a command, control, communications, computers, intelligence, surveillance, and reconnaissance (C4ISR) radio. The company traditionally used a design flow that relied on hand-coding FPGAs in VHDL®. They saw an opportunity to evaluate this approach against Model-Based Design and Xilinx tools.

BAE developed a model of the SDR transmitter and receiver in Simulink. They accelerated model development by incorporating blocks from Communications Toolbox™, including a scrambler, differential encoder, Reed-Solomon encoder, matrix interleaver, convolutional encoder, and quadrature amplitude modulation (QAM) modulator.

BAE handed the Simulink model off to a Xilinx engineer, together with a copy of the waveform specifications. Xilinx prepared the model for code generation by substituting Xilinx blocks for standard Simulink blocks.

After simulating and verifying the updated model, the Xilinx engineer used System Generator for DSP and Xilinx ISE to generate VHDL code for the SDR and deploy it to an FPGA for testing. Because the SDR design had been fully simulated and verified using the model, when downloaded to the FPGA, the implementation worked immediately.

4G: New RF and LTE Products, Advanced FPGAs

4G mobile telecommunications systems support data transmission rates of up to 100 MB per second and provide wireless device users with near-ubiquitous connections. With ever-changing specifications and standards, however, developing a prototype that proved the 4G system's capabilities required a flexible design process.

When 4G was ratified, Xilinx introduced the Kintex®-7 family of FPGAs, while MathWorks developed tools for simulating, analyzing, and testing the physical layer of LTE systems. MathWorks also introduced capabilities for generating VHDL or Verilog® code that can be used to program Xilinx FPGA devices.

Case Study: Electronics and Telecommunications Research Institute (ETRI)

> "The project would not have been successful if we had used a design method based on C. Model-Based Design with Simulink saved us a lot of time and helped us meet our deadline."
>
> — *Juyul Lee, ETRI*

The Electronics and Telecommunications Research Institute (ETRI) developed a prototype to prove the feasibility of an end-to-end, 4G, high-speed mobile telecommunications system. The system needed to maintain clear mobile connections for commuters taking public transportation, as well as high-speed data transmission to handle voice and video.

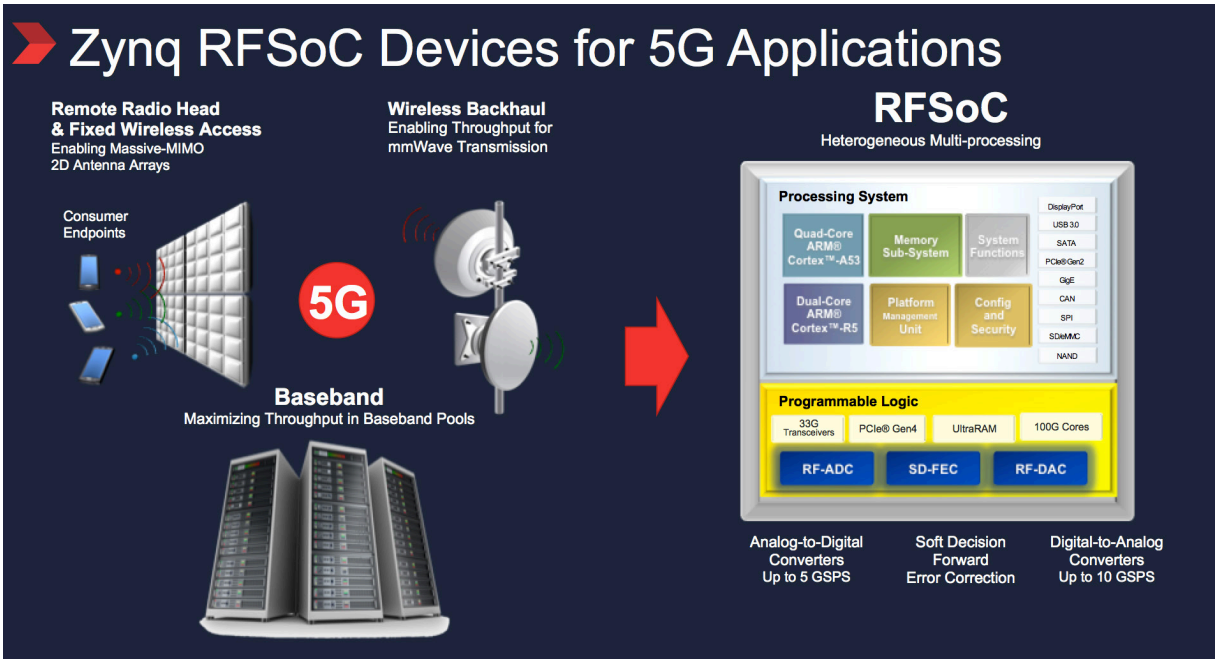
The most critical success factor was time: the entire development cycle, from algorithm development to system-level verification, had to be completed within a year to keep up with other research and commercial communications companies that were proposing 4G standards.

Using frame-based processing and the multirate sampling capabilities of Simulink and DSP System Toolbox™ enabled the ETRI team to model a system that was very close to the actual hardware implementation. They developed floating-point models in Simulink. Using Fixed-Point Toolbox™ and Simulink Fixed Point™, they then specified all the fixed-point data type properties of the design by modifying the floating-point models.

After completing the HDL coding for the receiver, ETRI used the fixed-point model as an executable specification to verify their code before implementation on a Xilinx Virtex-II FPGA. By using this approach, ETRI reduced development time by 50% over their previous C-based methods.

5G: Tackling Complex New Engineering Challenges

A standalone 5G wireless standard, approved in 2018, presented new engineering challenges. The 5G standard is much more complex than 4G because it introduces new capabilities like higher data rates, lower latencies, higher spectrum efficiency, and greater range, as well as new technologies such as multi-user massive MIMO, more advanced beamforming techniques, and faster mm wave transmission speeds with frequencies ranging from 30 to 300 GHz.



Xilinx introduced Zynq UltraScale+ RFSoC, a single-chip, adaptable radio platform for 5G and LTE Wireless. Zynq UltraScale+ RFSoC includes traditional FPGA fabric along with a processing subsystem with a quad-core ARM A53, real-time ARM R5, RF converters and forward error correction blocks, and a high-performance memory controller. To enable developers to design and deploy high-speed giga samples per second (GSPS) applications, Xilinx also added the Super Sample Rate (SSR) Simulink blockset to System Generator for DSP.

At the same time, MathWorks introduced a comprehensive set of tools for creating, optimizing, and implementing IP for 5G. These tools included standard-compliant functions and reference examples; support for end-to-end, link-level simulation and waveform generation and analysis; hardware-ready 5G and LTE subsystems; and blocks and visualization tools for modeling, simulating, and implementing hardware and software architectures for Xilinx FPGAs and SoCs.

Verification consumes a large proportion of a production project's schedule and resources. MathWorks introduced tools that streamline this process by enabling engineers to generate System Verilog components from MATLAB and Simulink for test and verification using HDL simulators and FPGA boards.

Case Study: Convida Wireless

> "It is not trivial to read and understand the standards and then build to the specifications. Having 5G Toolbox will help companies come up to speed quickly because the engineers can first verify their understanding of transmission. Then, if they want to build a receiver, for example, they have the complete transmitter chain available for simulation so they can focus on the receiver side."
>
> — *Lakshmi Iyer, InterDigital and Convida*

Convida Wireless is a joint venture between Sony Corporation of America and InterDigital that focuses on Internet of Things technologies and advancing the specifications and standards for 5G wireless technology. Convida is active in 3GPP Radio Access Networks working groups, RAN1 and RAN2, which involve collaborating with other delegates on defining robust 5G solutions and specifications.

The RAN1 group relies on simulations to evaluate proposed contributions to the standard. Submissions could include, for example, a PHY layer design with specific signal characteristics. The ability to perform both link-level and system-level simulation in MATLAB helped the group analyze capacity, throughput, and other network-level performance criteria.

In addition to participating in RAN 1 and RAN 2, InterDigital works on a number of projects that leverage commercial wireless technology. They use 5G Toolbox on those projects to better understand the performance and capacity gains that stem from 5G, which helps with planning future product lines.

Beyond 5G: Increasing AI Compute Power

With the rise of artificial intelligence (AI) and big data, developers are demanding ease of programming, higher performance, and adaptability. Traditional CPUs, GPUs, ASICs, and ASSPs are suitable for accelerating fixed functions, but rapidly changing algorithms are outpacing their evolution. Conventional FPGAs are the most flexible and highest performance accelerators, but up to now, they have required hardware skills to program.

Versal™ ACAP (Adaptive Compute Acceleration Platform), Xilinx's newest class of devices, is a fully software-programmable heterogeneous compute platform that includes scalar processing elements, vector processing elements, and programmable logic. Versal ACAP offers better performance than today's fastest FPGA and CPU implementations. The ACAP platform is dynamically customizable at the hardware and software levels to fit a wide range of applications and adapt to evolving algorithms and industry standards.

The Adaptive Intelligent Engines (AI Engines) on the Versal ACAP AI Core series have been optimized for DSP, AI technology such as machine learning and 5G wireless applications. AI Engines represent a new class of high-performance computing that offers high throughput and low latency while reducing nominal power consumption by up to 50%.

A Game-Changer

Combining Model-Based Design with FPGAs has been a game-changer for wireless infrastructure development for several reasons. MATLAB and Simulink offer a natural way to express parallelism and custom data paths between compute blocks before they are implemented on a specific FPGA. These tools support debug and test at the model level instead of at the RTL code level, which speeds up simulations by orders of magnitude and frees up time for performing what-if analyses and exploring algorithm trade-offs. MATLAB and Simulink make it possible to perform virtual testing on an entire system over a range of conditions, minimizing the number of downstream hardware iterations and hardware debug tasks. Lastly, they facilitate knowledge transfer by establishing an executable specification that can be used by all team members, whether they are FPGA engineers, RF engineers, or communications engineers.

For companies whose products cost thousands or millions of dollars, reducing the number of design iterations by just one is enough to provide a return on investment. Equally rewarded are companies with low-cost products and the potential for high market share if first to market. For them, the value driver of Model-Based Design and FPGAs is accelerated development. In both scenarios, companies achieve dramatic, ongoing benefits by using Model-Based Design with FPGAs for embedded systems development.

Ready for your teams to get started with Model-Based Design?

Contact fpga_expert@mathworks.com

Learn More

Simulation and Model-Based Design

MATLAB for Wireless Communications

Xilinx FPGAs and Zynq SoCs

Model Composer